"Minerva" Hardware for DFC

openHPSDR Forum Friedrichshafen, 25th June 2016

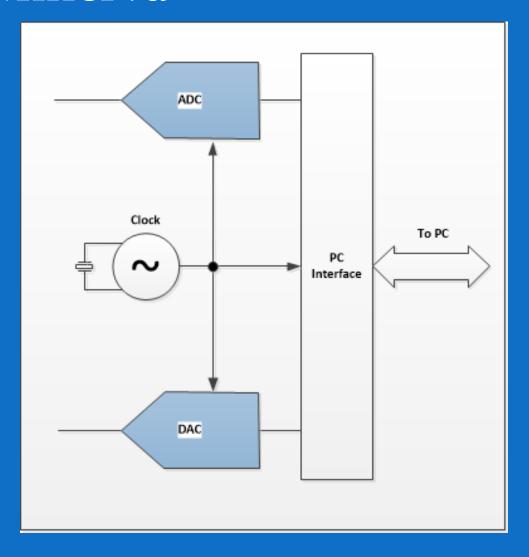
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DFC

- DFC is an alternative architecture for SDRs
- It moves all of the DSP to the PC
- Potential to provide high performance at low cost
- It can use Video GPUs and CUDA processing as a cost effective high performance DSP
- "Minerva" is the openHPSDR project name for hardware that supports DFC.
- Flexible architecture to provide simple integration of new devices

DFC

Basic Minerva

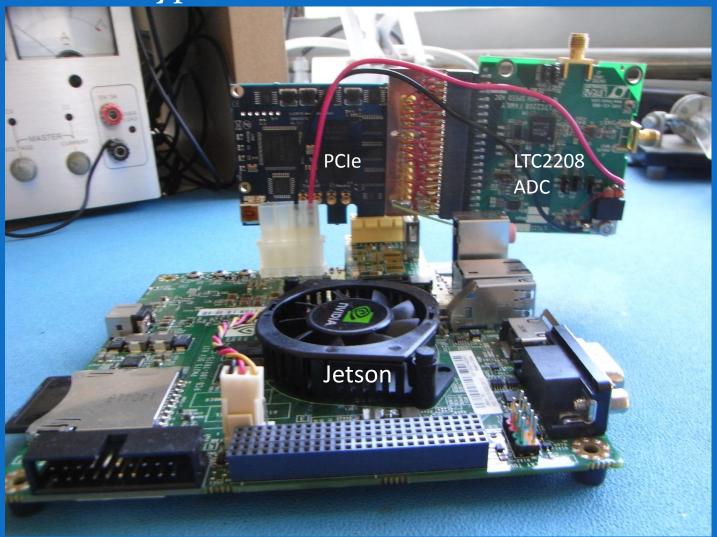


Direct Fourier Conversion

Implementation



DFC Prototype

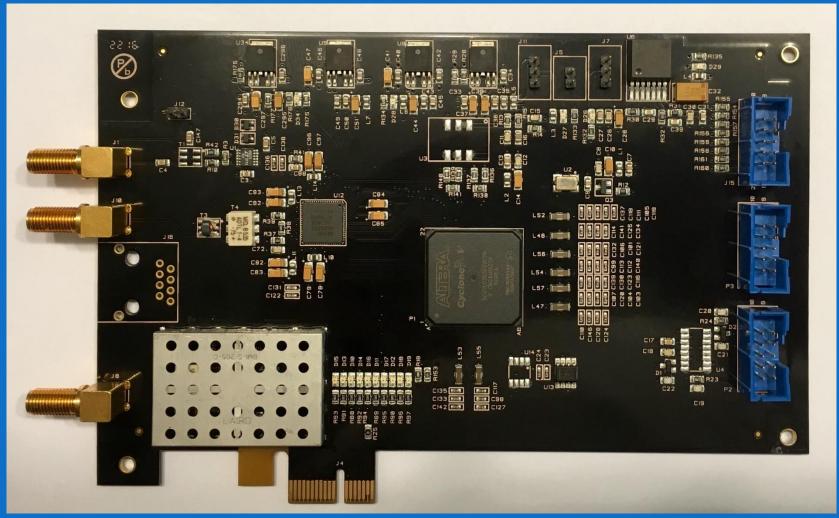


Minerva

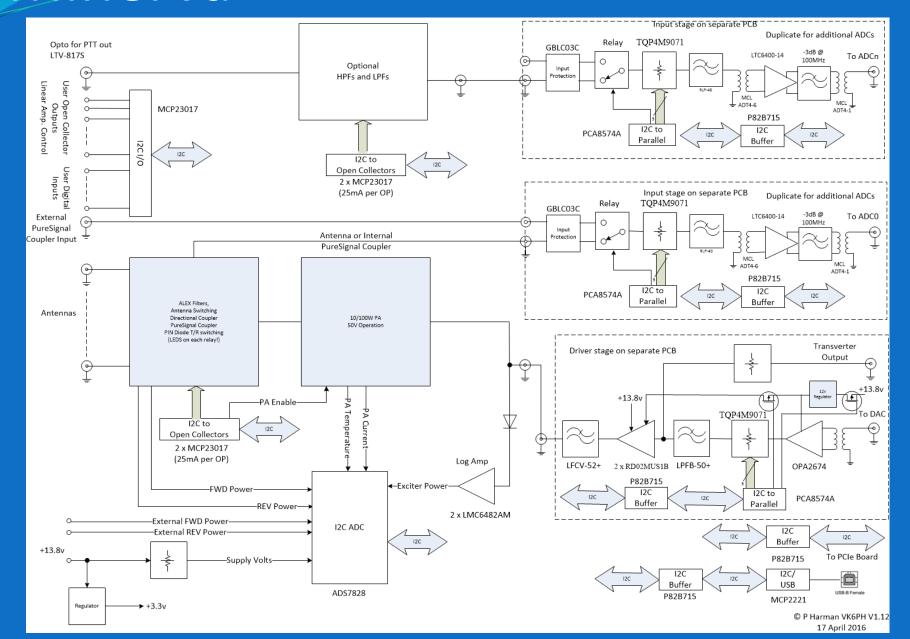
openHPSDR "Minerva" Duplicate for additional ADCs LTC6400-8 LVDS FIFO Max read 368MBps -ADC Clock--Overflow--Random-ADT1-8T -Dither-122.88MHz Crystek CVPD-922 PCIe Hardware IP EEPROM LVPECL **EPCSXXX** Programer PLL JTAG FIFO MAX5891 Max read 368MBps +3.3v -PCIe Gen 2 (5Gbps) 1 Lane (use p clock input) 10 MHz _Enable Max read 1MBps PLL –LVPECL–⋚ LTC6957-1 I2C Interface Data (RJ45) FIFO Max read 1MBps P82B715 Command Control EER/ET CYCLONE V GT FPGA Output1 +12V From PWM LEDs (RJ45) PCIe interface EER/ET Output2 +3.3V From PCIe interface SN74LVC2G126 SMPSUs in Screened Enclosure Spare I/O pins

Minerva

Photo of board



Minerva



Questions?