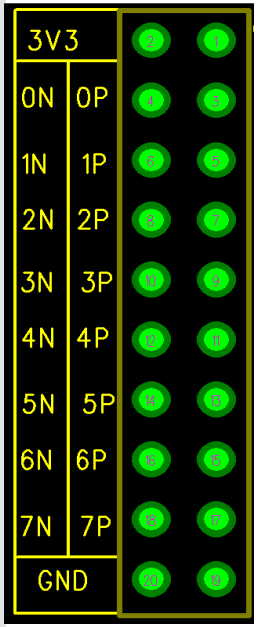
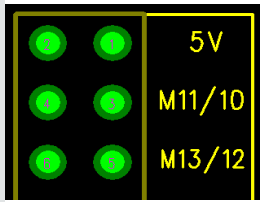
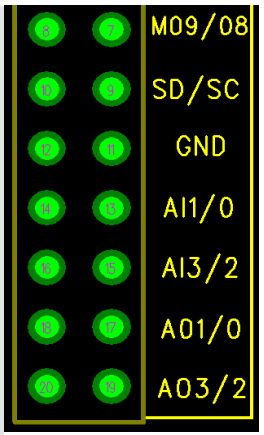
Pin	Description	FPGA pin number	FPGA pin description	Voltage levels
1	3V3			
2	3V3			
3	DIO0 P	G17	IO L16P T2 35 (EXT TRIG)	3.3V
4	DIO0 N	G18	IO L16N T2 35	3.3V
5	DIO1 P	H16	IO L13P T2 MRCC 35	3.3V
6	DIO1 N	H17	IO L13N T2 MRCC 35	3.3V
7	DIO2 P	J18	IO L14P T2 AD4P SRCC 35	3.3V
8	DIO2 N	H18	IO L14N T2 AD4N SRCC 35	3.3V
9	DIO3 P	K17	IO L12P T1 MRCC 35	3.3V
10	DIO3 N	K18	IO L12N T1 MRCC 35	3.3V
11	DIO4 P	L14	IO L22P T3 AD7P 35	3.3V
12	DIO4 N	L15	IO L22N T3 AD7N 35	3.3V
13	DIO5 P	L16	IO L11P T1 SRCC 35	3.3V
14	DIO5 N	L17	IO L11N T1 SRCC 35	3.3V
15	DIO6 P	K16	IO L24P T3 AD15P 35	3.3V
16	DIO6 N	J16	IO L24N T3 AD15N 35	3.3V
17	DIO7 P	M14	IO L23P T3 35	3.3V
18	DIO7 N	M15	IO L23N T3 35	3.3V
19	GND			
20	GND			



Pin	Description	FPGA pin number	FPGA pin description	Voltage levels
1	5V			
2	5V			
3	SPI(MOSI)	E9	PS MIO10 500	3.3V
4	SPI(MISO)	C6	PS MIO11 500	3.3V
5	SPI(SCK)	D9	PS MIO12 500	3.3V
6	SPI(CS#)	E8	PS MIO13 500	3.3V



7	UART(TX)	C8	PS MIO08	3.3V
8	UART(RX)	C5	PS MIO09	3.3V
9	I2C(SCL)	B9	PS MIO50 501	3.3V
10	I2C(SDA)	B13	PS MIO51 501	3.3V
11	GND			GND
12	GND			
13	Analog Input 0			0-3.3V
14	Analog Input 1			0-3.3V
15	Analog Input 2			0-3.3V
16	Analog Input 3			0-3.3V
17	Analog Output 0			0-1.8V
18	Analog Output 1			0-1.8V
19	Analog Output 2			0-1.8V
20	Analog Output 3			0-1.8V

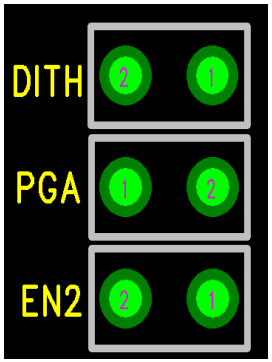


ADC control	
DITH	short to enable Internal Dither
PGA	short to set PGA =0

Internal Dither

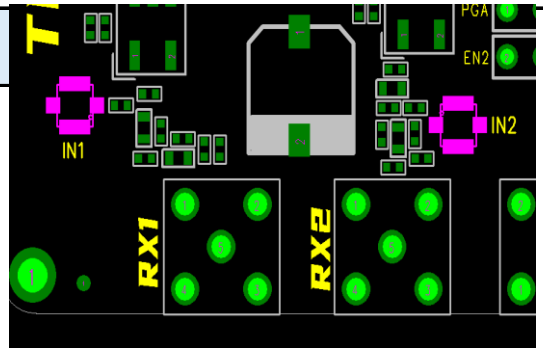
The LTC2208 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfec tions in the transfer function will result in unwanted tones.
Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

The **PGA** pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of 2.25VP-P; PGA = 1 selects an input range of 1.5VP-P. The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applica tions with high input frequencies, the low input range will have improved distortion; however, the SNR will be 1.8dB worse.

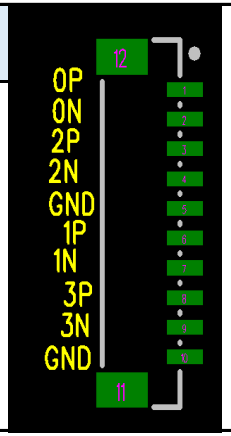


		worse
EN2	short to disable ADC2	Can reduce 1.2W power consumption and reduce heat generation

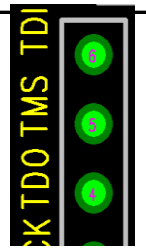
IN1&2	Bypass the input LowpassFilter of ADC1&2,can use to undersampling



	Daisy chain connector (up to 500 Mbps)
0P	IO_L2P_T0_34
0N	IO_L2N_T0_34
1P	IO_L11P_T1_SRCC_36
1N	IO_L11N_T1_SRCC_36
2P	IO_L6P_T0_34
2N	IO_L6N_T0_34
3P	IO_L13P_T2_MRCC_34
3N	IO_L13N_T2_MRCC_34



JTAG PORT 3.3V level




3V GND TC
3
2
1