AMPLEON

Extremely Rugged 50 V LDMOS Devices Capture ISM and Broadcast Markets Whitepaper

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During the last two and a half decades, VDMOS transistors have been the workhorses in many ISM and broadcast applications. Now, that era has come to an end due to continuous improvements in Ampleon's 50 V LDMOS technology. The BLF18x-XR series of LDMOS devices enables superior reliability and lower system cost, while eliminating the need for hazardous substances associated with VDMOS packages. This new XR series has been specifically designed for RF energy applications in the industrial, scientific and medical (ISM) frequency bands, where ruggedness, stability and reliability are key drivers both in the market and in transistor design. The devices also enable high efficiency FM and VHF-TV broadcast transmitters with superior correctable linearity.

Ampleon's customers now have access to a portfolio of devices that will meet all design challenges in today's applications based on continuous wave, pulsed or linear systems. This paper gives an in-depth description of the technology's features and how they relate to the performance improvements obtained. Application examples will be given using our latest 50 V LDMOS devices, which provide superior performance when compared to older VDMOS and other 50 V LDMOS technologies currently available in the market.

High Voltage LDMOS Technology

Ampleon's extremely rugged 50 V transistors are processed in an 8-inch CMOS-wafer fab, which has lithography capabilities down to 0.14 µm. The LDMOS process is derived from the C075 CMOS (0.35 µm gate) process with LOCOS isolation. Additions to the C075 process are the source sinker to the substrate, CoSi2 gate silicidation, tungsten shield and mushroom-type drain structure with thick multi-layer AlCu metallization. **Figure 1** is a cross section of the VDMOS technology, and **Figure 2** shows the cross section of an LDMOS transistor.

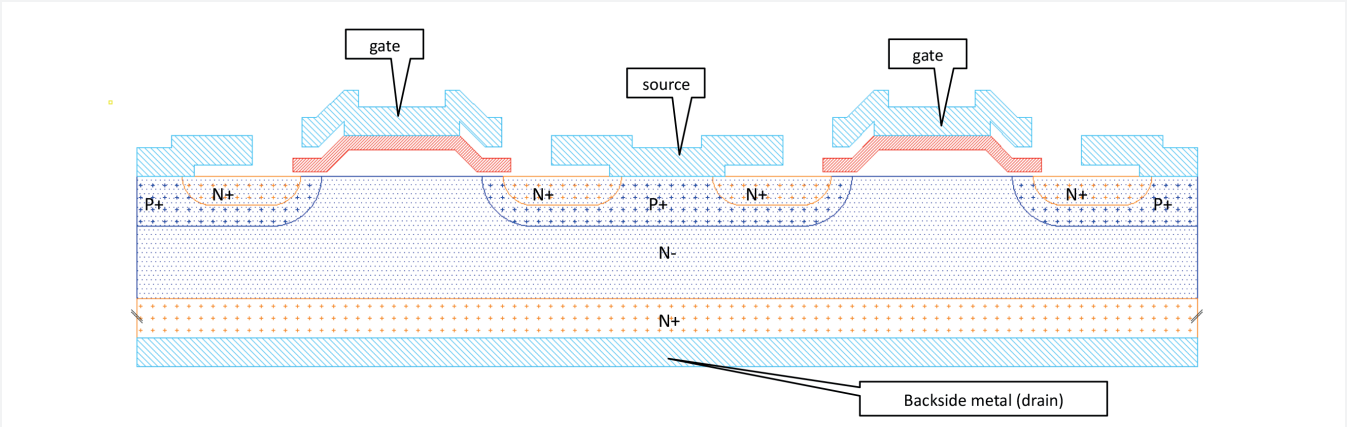


Figure 1: Cross-section of a vertical DMOS transmitting transistor. The length of the gate (the channel length) is the plane of the paper, the channel width is into the plane of the paper.

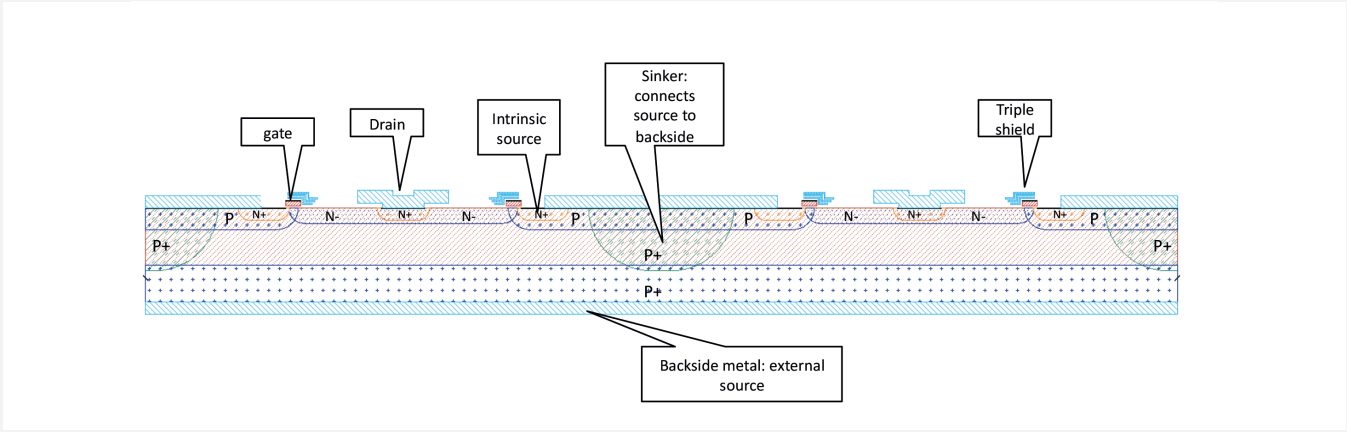


Figure 2: Schematic cross-section of a state-of-the art LDMOS transistor.

There are a number of important differences between the transistors. With a VDMOS transistor the current flows vertically from top to bottom, the backside of the die is the drain, and a high supply voltage will be present during operation. With an LDMOS transistor, the current flows laterally. The source is connected with a P+ sinker to the backside of the wafer, which makes the backside of the die the source connection of the transistor. The lateral construction enables optimization for high voltage operation at RF frequencies by proper drain-engineering. Appropriate doping levels are chosen in combination with the construction of a field plate, using the "resurf" effect **[1]**. In addition to drain engineering, optimization of the parasitic bipolar was carried out **[2]**, and will be discussed later in this paper.

Technology Comparison

Table 1 shows a comparison between VDMOS (Ampleon's BLF278), Ampleon's BLF188XR LDMOS transistor and a competitor device.

Parameter	BLF188XR LDMOS	Competitor LDMOS	BLF278 VDMOS	Unit
Rated POUT (f = 88 - 108 MHz, coaxial match)	1250 CW	1100 CW	300 CW	W
Power Density	+++	++	+	-
Power Gain (f = 88 - 108 MHz, coaxial match)	24.5	25.0	18	dB
Drain Efficiency (f = 88 - 108 MHz, coaxial match)	83.6	79.2	80	%
Thermal Resistance (RTH, J-C)	0.1	0.15	0.35	K/W
BVDSS	>135	>133	>125	V
On-die Integrated stability network	Yes	Yes	No	-
Ruggedness	+++	+++	+++	-
Avalanche Energy Datasheet Specification	Yes	No	No	-
ESD-Diode	-6 to +11	-6 to +10	No	V
ESD Class 2 HBM	6000	3500	-	V
Long Term Reliability (TTF)	+++	+++	++	-
Corrected Linearity for VHF-TV	++	++	++	-
Technology Maturity	Excellent	Excellent	Excellent	-
Toxic BeO in Package	No	No	Yes	-

Table 1: Comparison LDMOS and VDMOS

In the paragraph below a discussion about the relevance of the various parameters in **Table 1** in relation to the various applications is given. We can distinguish between two application areas:

- ISM, high to very high power levels, often exposed to high mismatch where stability, ruggedness and reliability are key design parameters
- Broadcast, high to very high peak power levels, where efficiency and exciter corrected linearity are key design parameters

Thermal Resistance

Thermal resistance is the key parameter that is designed to be as low as possible in order to:

1. Ensure low die junction temperatures to ensure long term reliability (TTF)
2. Maximize the power dissipation the device can handle during mismatch conditions. High currentconditions, and thus high dissipation, can occur depending on the application circuit design and the phase angle of the mismatch. This can create very high dissipation levels, which may result in thermal breakdown of the die and transistor. This typically causes complete destruction of the transistor, see **Figure 3**.

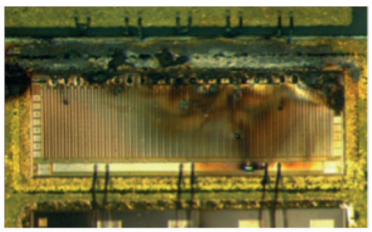


Figure 3: Example of a thermal device failure as a result of high dissipation

Generally the thermal resistance can be divided into an $R_{TH,J-C}$ (junction to case) part and an $R_{TH,C-HS}$ (case to heat sink) part. The $R_{TH,J-C}$ is specified by the device manufacturer and the $R_{TH,C-HS}$ depends on the material stack used in the circuit design.
A typical setup to measure the thermal resistance is shown in **Figure 4**.

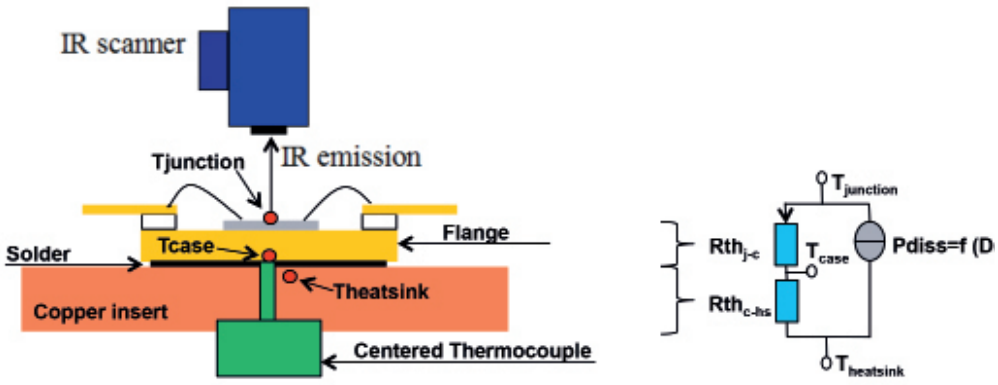


Figure 4: Typical infrared measurement setup

The setup has an infrared (IR) camera located directly above the device capable of capturing an enlarged junction temperature image of sections of the device. The device is soldered on a copper insert which is clamped between the input and output part of the test circuit. This total system is then clamped on a water-cooled plate. In order to determine the $R_{TH,J-C}$, the following information is gathered during the measurement.

$$R_{TH,J-C} = \frac{T_J - T_C}{P_{DISS}(Eff_D, P_{OUT})} \quad \text{[Equation 1]}$$

The dissipated power (P_{DISS}) is a function of drain efficiency (Eff_D) and the RF output power (P_{OUT}). Thermal resistance of a VDMOS transistor is relatively high compared to an LDMOS product as shown in **Table 2**.

	BLF188XR LDMOS	BLF184XR LDMOS	BLF278 VDMOS
$R_{TH,J-C}$ [K/W]	0.1	0.18	0.35

Table 2: Comparison $R_{TH,J-C}$ LDMOS vs VDMOS

Amongst other reasons, the relatively high $R_{TH,J-C}$ of a VDMOS device is caused by needing an insulating BeO-disk to mount the VDMOS die (back side is the drain which carries the 50 V supply voltage). This increases the $R_{TH,J-C}$. The thickness of the die also plays a role in the overall R_{TH}. The VDMOS die is about 200 µm thick, as die lapping techniques were not as advanced when the technology was developed. The LDMOS dies, which are also thinner (120 µm) when compared to VDMOS, are mounted directly to the metal flange of the transistor using a eutectic die attach. This eliminates the need for a thermal interface, thus ensuring the lowest possible thermal resistance for LDMOS devices. The layout of the active die areas and pitch between the fingers of the die have been designed for an optimum thermal resistance and temperature profile along the die, as examined during the IR results shown in **Figure 5**.

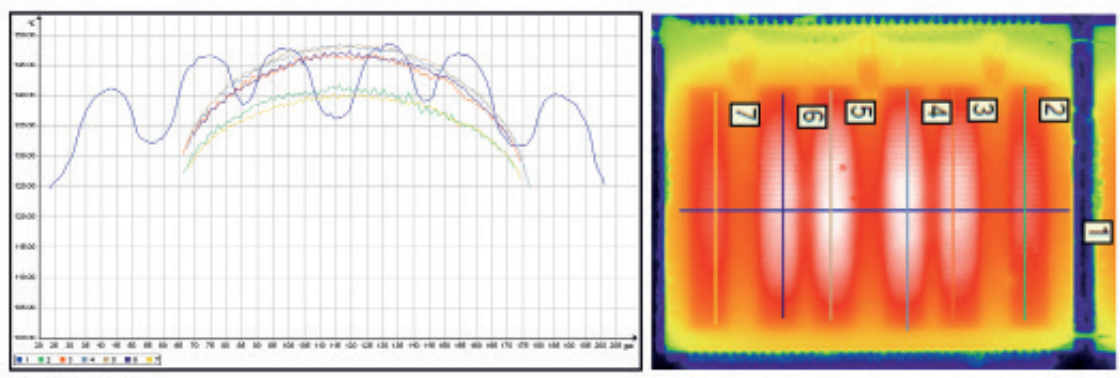


Figure 5: BLF188XR Infrared temperature profile

The thermal resistance, sometimes referred to as thermal impedance (Z_{th}), of an LDMOS transistor changes as a function of pulse width (t_{pulse}) and duty cycle (dc). These thermal properties (as a function of pulse width and duty cycle) are recorded during the IR measurements. **Figure 6** shows the results for the changes in thermal impedance Z_{th}, where dc = 1 corresponds to continuous wave (CW) operation.

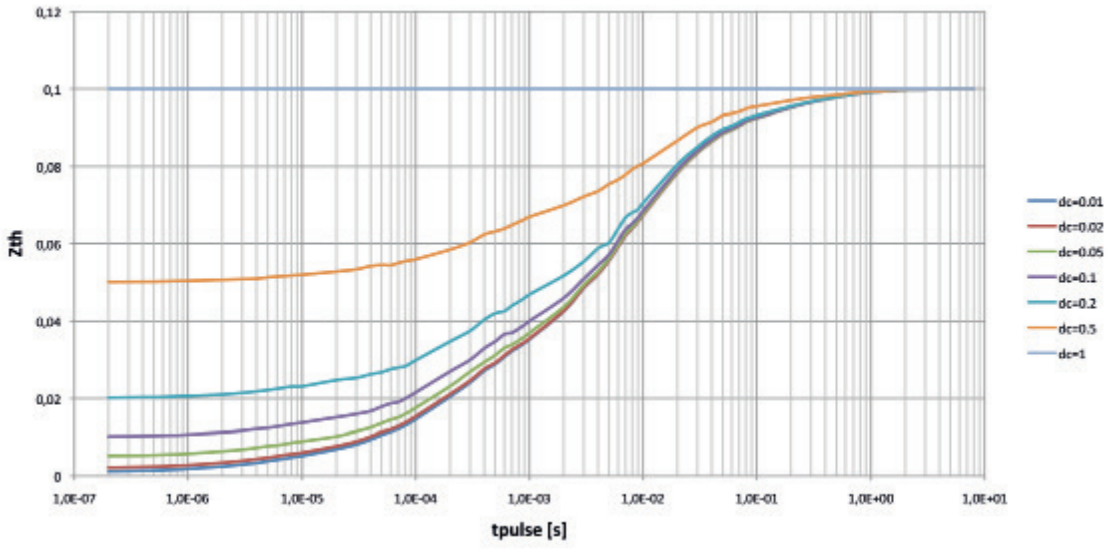


Figure 6: Thermal impedance (Z_{th}) for the BLF188XR as a function of pulse width and duty cycle

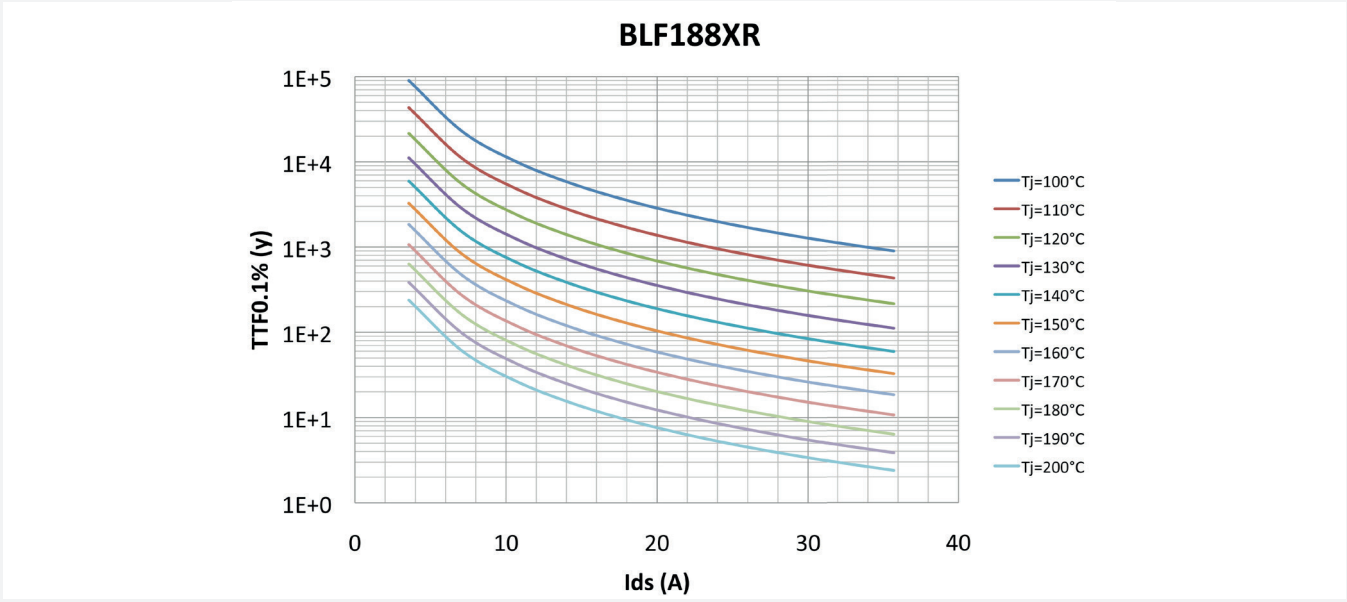


Figure 7: BLF188XR TTF curves for 0.1% failure fraction as function of DC current and temperature

A low thermal resistance is important to ensure long-term reliability of the LDMOS device. **Figure 7** shows the lifetime in years at 0.1% failure fraction ($TTF_{0.1\%}$) for the BLF188XR as a function of the junction temperature and the drain-source (i.e. supply) current I_{DS}. $TTF_{0.1\%}$ should not be confused with $MTF_{50\%}$, which will show much more optimistic figures.

BVDSS (Vertical Breakdown Voltage)

BV_{DSS} is an important transistor design parameter and influences power capability and ruggedness: in particular when there is significant harmonic content in the output voltage waveform. From theory it is known that the output current waveform has significant 2nd harmonic content when the internal current source is terminated with a non-zero 2nd harmonic impedance. The resulting 2nd harmonic voltage adds to the fundamental waveform and limits the headroom of the fundamental output voltage, thus limiting the RF output power. This effect is shown in **Figure 8** for a 108 MHz test circuit with significant harmonic content, i.e. non optimal harmonic termination at circuit level.

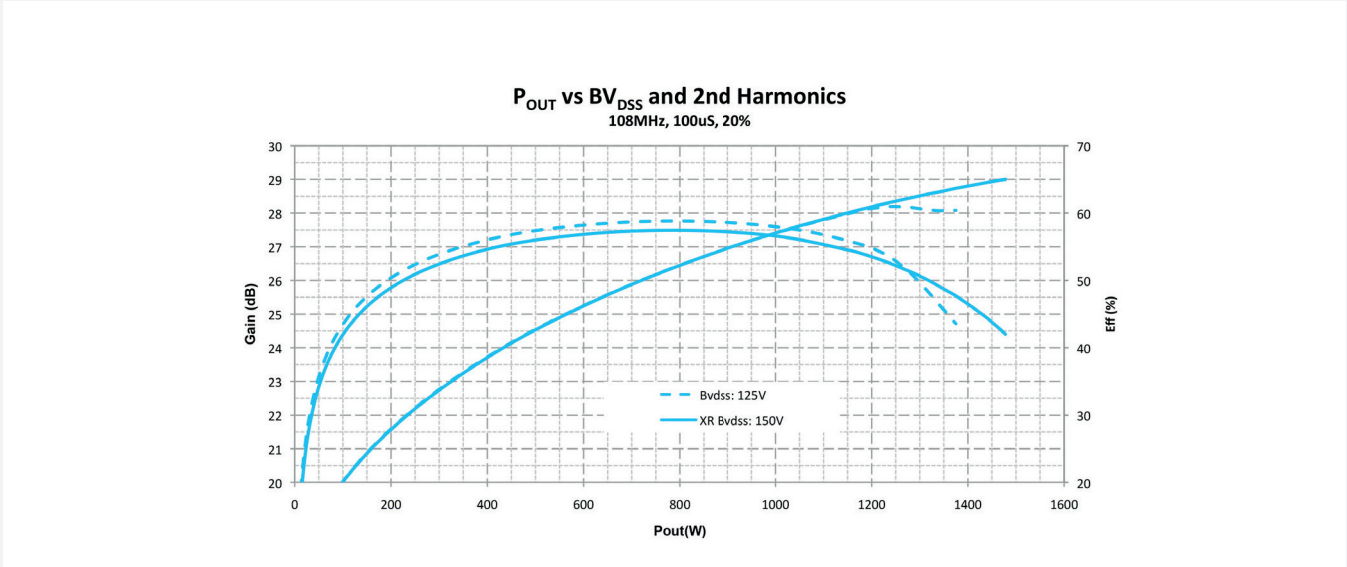


Figure 8: A higher BV_{DSS} in the case of a high harmonic content improves the output power and efficiency when the device starts to compress

Two transistors are compared. The first one has a typical BV_{DSS} of 125 V (dashed line) and the other with a typical BV_{DSS} of 150 V (solid line). It can be seen that the device with the 125 V breakdown voltage goes into compression faster. The obtainable output power is lower and, because the transistor goes into avalanche the efficiency is also affected at output power levels close to compression. The benefits of a transistor with a high BV_{DSS} are even greater when the device is tuned for efficiency (high load-line), used in high classes of operation, or when severe mismatches are applied. Depending on the application design, and as a function of the mismatch phase angle, high voltage peaks may occur on the die, which can lead to degradation or destruction of the transistor. It is obvious that for lower operating frequencies, the effect of higher order harmonics becomes more significant and a high BV_{DSS} is more important. The BLF18x-series has a high BV_{DSS}, as determined by the resistivity and thickness of the epi-layer.

Parasitic Bipolar Breakdown

A parasitic NPN transistor is inherently present in every LDMOS transistor, as part of its structure. **Figure 9** gives the schematic representation of the LDMOS transistor, including the parasitic NPN transistor and the drain-substrate diode. **Figure 10** highlights the location of the parasitic bipolar NPN transistor in the LDMOS structure.

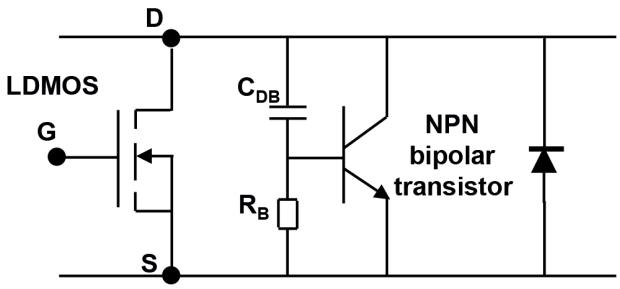


Figure 9: Electrical representation of the LDMOS and the inherently present parasitic bipolar transistor and drain-substrate diode

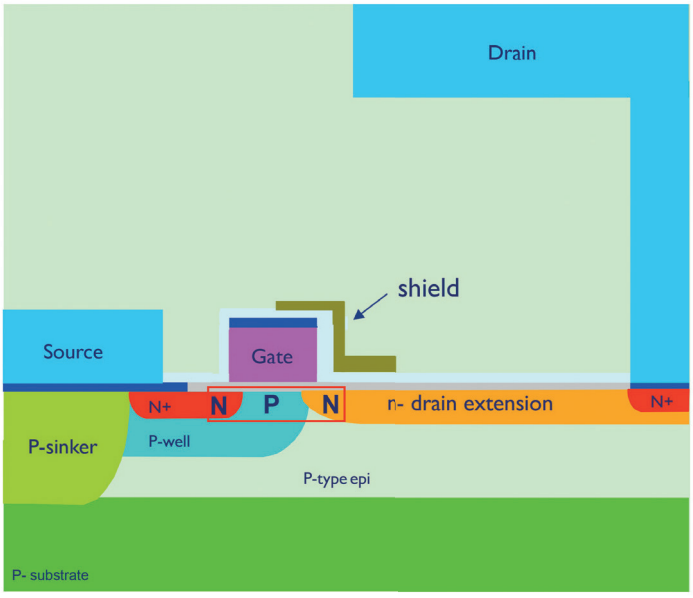


Figure 10: Parasitic bipolar NPN transistor highlighted in the LDMOS structure

The drain-source diode clamps the voltage across the LDMOS and the parasitic bipolar sinks the excess current to the substrate. For large sink currents, however, the drain-source voltage exceeds the diode breakdown voltage and the parasitic bipolar transistor can be triggered. Large sink currents can be caused by a mismatch event, improper termination of harmonics, or operation in saturation. Triggering of the parasitic bipolar will lead to nearly instantaneous failure of the LDMOS transistor, an example is shown in **Figure 11**. This shows that the failure signature only shows a couple of burned fingers, whereas **Figure 3** shows much greater destruction when the transistor goes into thermal failure.

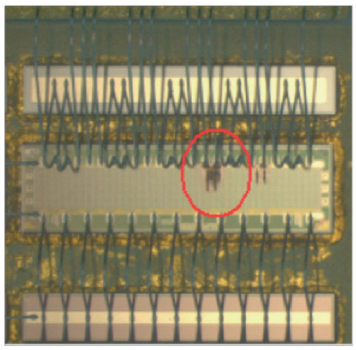


Figure 11: Transistor failure signature when the parasitic bipolar transistor has been triggered

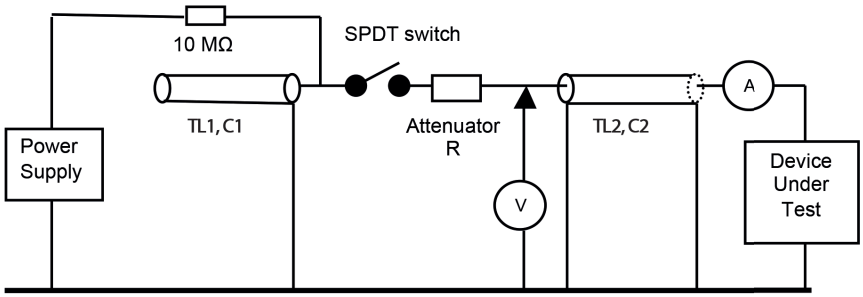


Figure 12: Pulse shaping network for TLP test methodology

To make the parasitic bipolar transistor more robust for a triggering event, it has been characterized by a TLP (Transmission Line Pulse) measurement and optimized. The TLP-test is an on-wafer characterization method (see **Figure 12**) to determine the triggering characteristics of the parasitic bipolar in the LDMOS device. With a short pulse (50 to 200 ns) the "snap-back" I-V characteristic is measured. The pulse shaping C1-R-C2 network formed by TL1, the attenuator TL2 and the 50 Ohm cable to the device under test, is chosen to set the desired pulse rise time, duration and fall time. The supply voltage determines the peak test voltage applied to the device under test. Important parameters to optimize are the base resistance R_B (see **Figure 9**), the gain and the maximum base current of the parasitic bipolar NPN transistor. Once an LDMOS transistor fails, because of a triggered parasitic bipolar, the device often exhibits a low gate-source resistance (< 200 ohms) when measured with an Ohm-meter on the gate of the device. A perfectly good device will show a very high gate-source resistance (> 1 megaohm). Improved drain engineering together with optimizing the robustness of the parasitic bipolar has resulted in Ampleon's extremely rugged 50 V LDMOS technology.

On-die Stability Network

Stability and spurious performance are of particular importance when the device is exposed to severe load mismatch conditions. Stability is important for ISM applications where stringent spurious requirements (< -50 dBc) need to be met.

When the transistor is potentially unstable, and when exposed to severe mismatch conditions, spurious products falling above the specification limit can occur. The BLF18x-XR series has on-die stability networks that minimize stability problems. These internal networks, together with a proper application design, will minimize transistor degradation or destruction. The stability measures that need to be taken in application circuit designs with the BLF18x-XR series are much less severe compared to earlier high voltage LDMOS generations, and in some cases can be completely eliminated. For the LDMOS transistor to accomplish this, an on-die RC network is integrated on the gate side of the transistor, involving large capacitance values of several hundred picofarads. This on- die capacitor is realized using a MIM-cap (Metal-Insulating-Metal capacitor) with nitride dielectric. To guarantee lifetime reliability, Ampleon performs on-die screening of the integrated MIM-caps **[3]**. Ampleon is the only company in the industry that has enabled on-die screening for its extremely rugged LDMOS technology, which further enhances the reliability of its transistors.

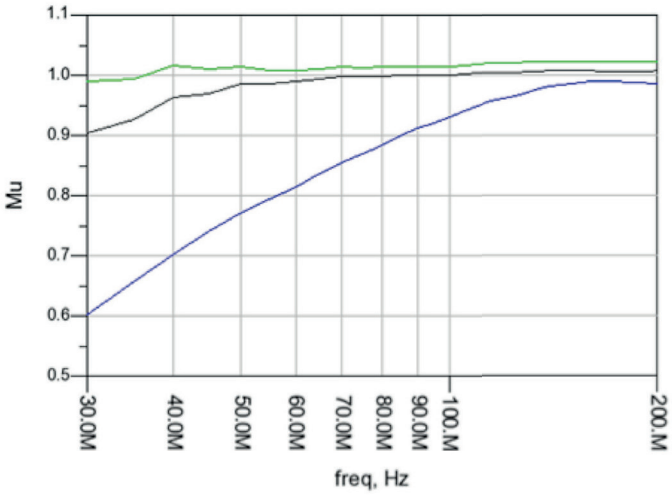
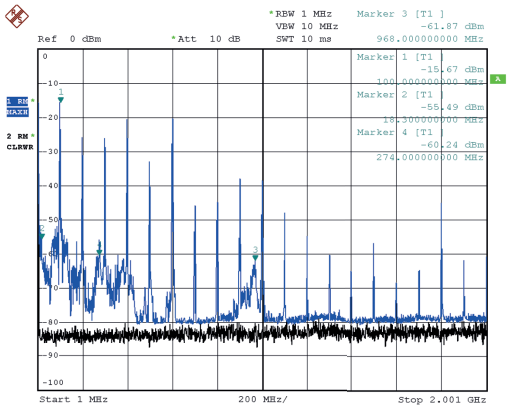


Figure 13: Stability (Mμ-factor) for the BLF188XR (green line), a competitor LDMOS device (black line), and the BLF278 VDMOS transistor (blue line)

Figure 13 shows that the BLF188XR is unconditionally stable (Mμ > 1) down to 40 MHz. Below 40 MHz the device is potentially unstable. In such a case stability measures may need to be implemented at circuit level outside the transistor. The competitor device and the BLF278 VDMOS transistor show a less than desired Mμ-factor. Die layout also plays an important role in device stability. An improper die layout can even lead to power scaling issues as a result of oscillations. A transistor with stability problems also risks a lower ruggedness performance.



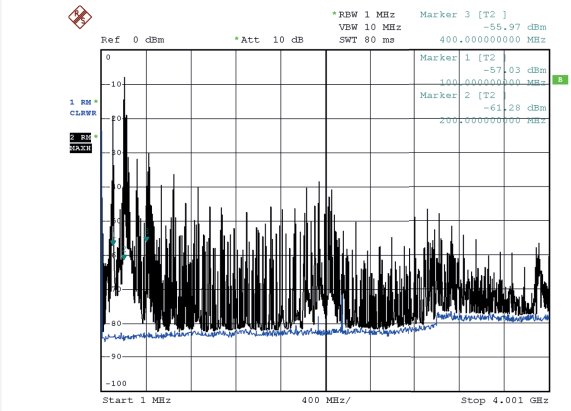


Figure 14: Spectral plot of the BLF188XR (left) and a competitor LDMOS transistor (right) under severe mismatch conditions

Figure 14 shows the spectral purity of the BLF188XR versus a similar competitor LDMOS transistor under the same mismatch conditions and in the same application circuit. The spurious products are minimal in the left plot (BLF188XR), and merely harmonics are shown which can easily be filtered out. The plot on the right (competitor device) shows a much less clean spectrum, without the ability to filter out the spurious products around the carrier.

Ruggedness

Ruggedness of an RF Power transistor is a complex topic. When an LDMOS transistor is exposed to severe mismatch conditions it can be partly damaged, which can result in performance degradation, or in the most extreme situation, the transistor can blow up (see **Figure 3** and **Figure 11**).

Transistor ruggedness is determined by:

- BV_{DSS}
- Breakdown characteristics of the parasitic bipolar transistor
- Power dissipation that the transistor can handle
- Intrinsic transistor stability (see previous paragraph)
- Avalanche energy that the transistor can handle

There are two ways to characterize the ruggedness of a transistor:

- A high VSWR test, using a mismatch unit with a pulsed CW signal, while increasing the supply voltage
- V_{DS}, the RF output power P_{OUT} and manipulating the rise/fall time of the pulse
- Determine the avalanche energy of the transistor using an Unclamped Inductor Switching (UIS) test

High VSWR test

Determining transistor ruggedness by applying a mismatch to the application circuit is achieved by connecting a phase unit to the test circuit.

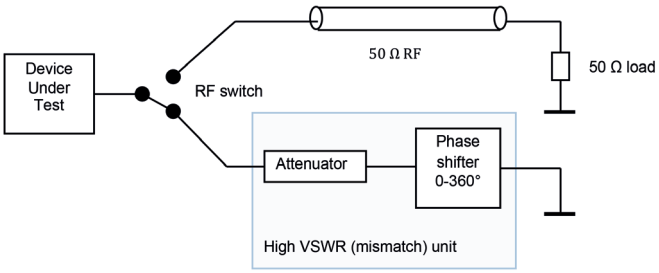


Figure 15: Block diagram ruggedness testing with mismatch unit

The applied VSWR can be reduced by adding an attenuator in front of the phase unit. The resulting VSWR is calculated with the following formula, where S is the desired VSWR.

$$Attenuation = 10 \log \frac{S+1}{S-1} \qquad \text{[Equation 2]}$$

To achieve a VSWR = 10:1, the required attenuator in front of the (ideal) phase shifter is 0.8715 dB. Please note that it is extremely difficult to create a phase unit with an infinite VSWR for all phases. Any loss in the phase unit results in a reduction of the VSWR from infinity. Typically, the VSWR of a phase unit varies as a function of the phase angle, and a good (practical) phase unit has VSWR values between 65 and 100. To test the ruggedness as determined by the BV_{DSS} and the parasitic bipolar, typically a pulsed CW signal is used. This avoids transistor break-down at maximum allowable dissipation P_{DISS}. The maximum dissipated power due to reaching power dissipation limits can be calculated using the maximum junction temperature ($T_{J,MAX}$ for the BLF188XR is 225 °C) and the thermal resistance.

$$P_{DISS} = \frac{\Delta T}{R_{THJ-C}} \qquad \text{[Equation 3]}$$

For a case temperature of 75 °C under CW conditions, the maximum dissipated power is 1500 W for an $R_{TH,J-C}$ of 0.1 K/W. Typical pulse conditions used at Ampleon are 50 or 100 µs with 10% duty cycle. Fast rise and fall times, in combination with high drain currents and high inductor values in the application circuit, may have a negative impact on the ruggedness because they can generate high voltage spikes arising from L(dI/dt) transients. However, the breakdown voltage of the parasitic bipolar appears to be sufficiently high for most real-world situations. At Ampleon, high VSWR ruggedness testing starts at nominal supply voltage and nominal output power with a VSWR > 65:1 (through all phases). After the devices pass that test, input drive is gradually increased to levels where the device is 5 dB in compression. Once that test is passed, it is repeated, but now at increased supply voltage. **Table 3** gives the tests results for the BLF184XR and BLF188XR, for supply voltages (V_{DS}) up to 60 V.

BLF184XR					
V_{DS} (V)	RF Output Power Test Level (Watts)				Result
50	-	600	650	700	Pass
55	-	600	780	820	Pass
60	-	800	925	970	Pass

BLF188XR					
V_{DS} (V)	RF Output Power Test Level (Watts)				Result
50	1100	1200	1300	1400	Pass
55	1300	1500	1600	1700	Pass
60	1600	1800	1900	2000	Pass

Table 3: High VSWR (>65:1) test results BLF184XR and BLF188XR
Test conditions: Pulsed CW; Pulse Width = 50 µs, Duty Cycle = 10 %, f = 100 MHz, VSWR > 65:1

UIS Test to Determine Ruggedness

The UIS test was developed for testing avalanche dependability of switch mode power supply MOSFETS. Power MOSFET devices are rated for a certain maximum BV_{DSS} reverse voltage, and operation of devices at V_{DS} well above the BV_{DSS} breakdown threshold causes the creation and multiplication of electron-hole pairs. This reverse avalanche current flows through the drain-substrate pn-diode causing high dissipation, which leads to thermal destruction. The UIS test determines E_{AS}, the amount of avalanche energy the device can dissipate and absorb in the pn-diode structure. The UIS test is not performed with the device at nominal bias conditions.

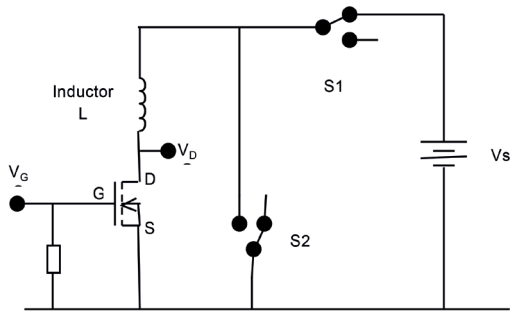


Figure 16: Schematic representation of the Unclamped Inductive Switching (UIS) test setup

A simplified schematic of the UIS tester is shown in **Figure 16**. At the start of the test, switch S1 is closed and the gate of the DUT is energized with a V_{GS} = 10 V (device fully open). The drain current will increase linearly (T1 period, see **Figure 17**). The instantaneous current is measured with a wideband current probe (not depicted in the diagram). When the drain current reaches the programmed maximum peak current the DUT is turned off by lowering the gate voltage to 0 V and S1 opens, removing the drain power, and closing S2. Current in the inductor continues to flow and causes the voltage across the DUT to

rise until the avalanche breakdown voltage is reached. The device begins conducting in avalanche and dissipates the energy that was stored in the inductor. If the device can handle the dissipation, the current decays linearly (T2 period, see **Figure 17**) until the energy is fully depleted.

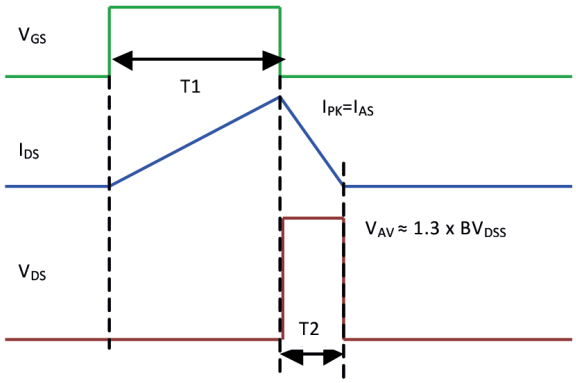
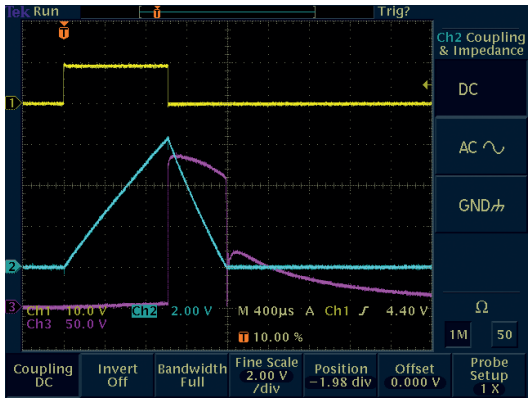


Figure 17: Timing diagram of avalanche breakdown test
T1 depicts the charging of the inductor. T2 depicts the avalanche phase

After this the inductor value L is increased to a higher value and the process is repeated until the avalanche voltage VAV breaks down during the T2 period. Upon this event the test is stopped. Now the applied energy, and thus the absorbed single pulse avalanche energy E_{AS}, can be calculated (**Equation 4**) for the chosen maximum test current IAS.

$$E_{AS}\,(J) = \tfrac{1}{2} \times L \times I_{AS}^2 \qquad \text{[Equation 4]}$$

Figure 18 shows avalanche waveforms for the BLF184XR at an avalanche current of 25 A. The left picture shows the last test before avalanche breakdown happens. The right picture shows avalanche breakdown during T2.



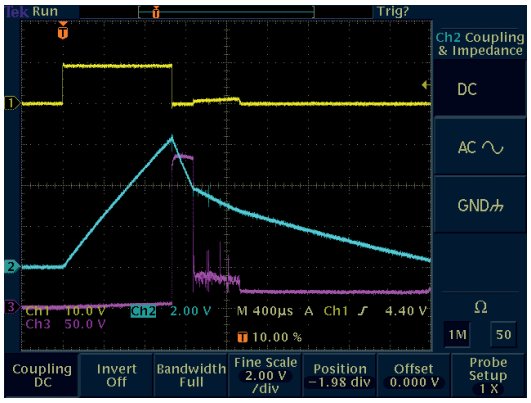


Figure 18: BLF184XR avalanche waveforms just before and during avalanche breakdown

A summary of the avalanche test results using the UIS tester, performed on the BLF278 (VDMOS) and BLF184XR and BLF188XR, can be found in **Figure 19**. Note that the figures below are for a single section of these push-pull transistors.

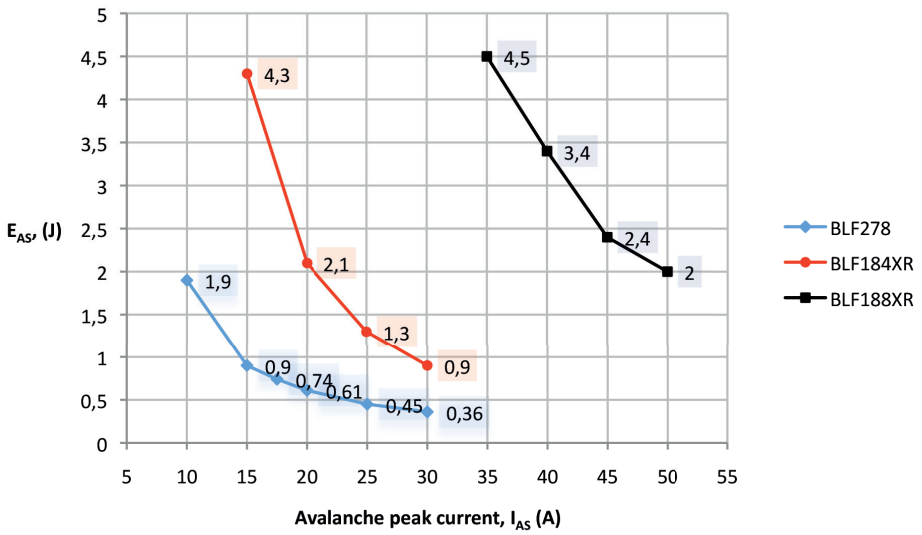


Figure 19: Avalanche test results for the BLF278, BLF184XR and BLF188XR for a single transistor section

ESD Diode Enhancement

VDMOS devices did not have any ESD diode protection on the gate side of the transistor. Older 50 V LDMOS devices such as the BLF178P, used a single-sided ESD diode to protect against ESD events on the gate. This single-sided ESD diode had a specification of -0.5 to +11 V. Depending on the application and the application circuit design, it is possible that when the negative cycle of the RF waveform exceeds -0.5 V, the single-sided ESD diode starts to conduct and act as a rectifier (see **Figure 20**).

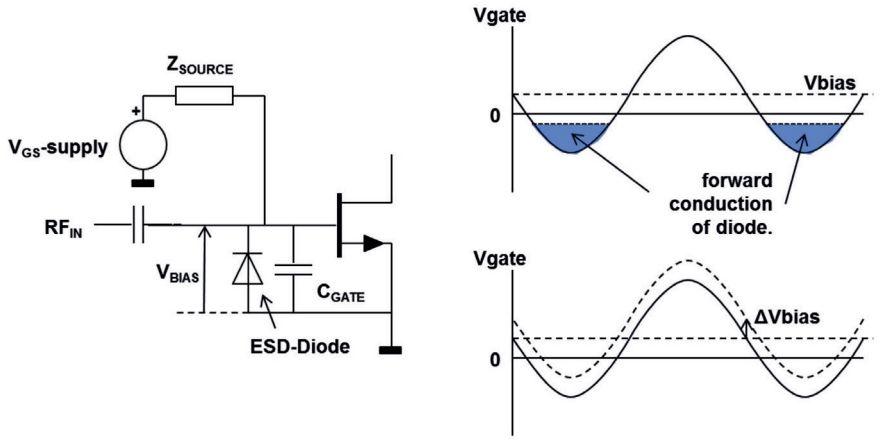


Figure 20: Single-sided ESD diode can cause shift in V_{BIAS}

The amount of rectification is determined by the speed and duration of the signal (pulsed signals and digitally modulated signals have less impact than CW signals). It is also determined by the source impedance (Z_{SOURCE}) of the gate bias (V_{GS} supply) circuit. A high source impedance results in more ΔV_{BIAS} (see **Figure 20**). A change in V_{BIAS} causes a shift in the operating point of the transistor and can change the mode of operation from Class-C to Class-AB, or even more severe, to Class-A operation. **Figure 21** shows the degradation in efficiency at high compression levels for a product without an ESD diode and a product with a single-sided ESD diode.

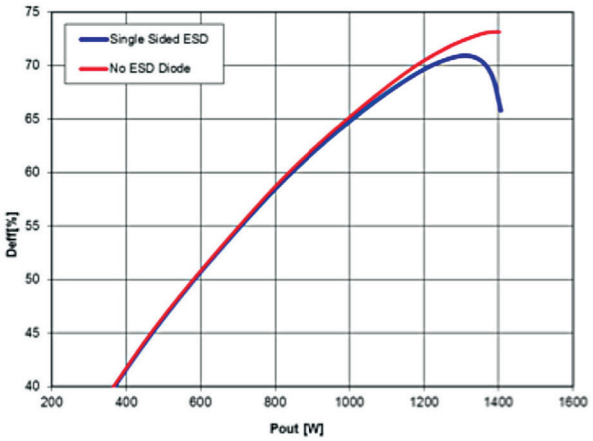


Figure 21: Degradation of drain efficiency as a result of a VBIAS shift when the single sided ESD diode is present.When there is no ESD diode present, a V_{BIAS} shift will not occur (no rectification)

It is always recommended to have a low Z_{SOURCE} for the V_{GS}-supply. Ampleon typically uses a circuit with a low source impedance. The schematic diagram of this circuit can be found in **Figure 22**. A detailed description of this V_{GS}-supply circuit can be found in **[4]**.

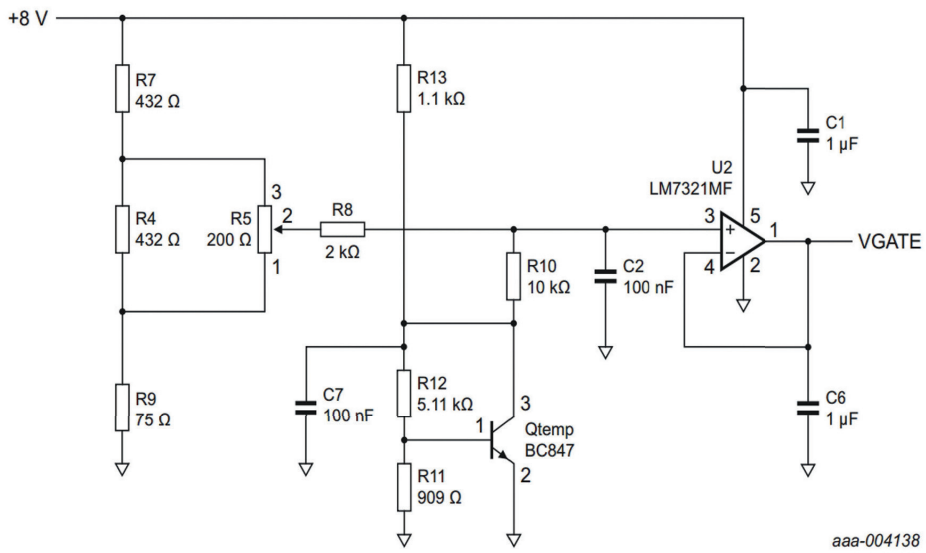


Figure 22: Low Z_{SOURCE} gate bias circuit

The BLF17x-XR series and BLF18x-XR series use a 'dual-sided' ESD diode structure (see **Figure 23**) with limiting values of -6 to +11 V. On the left the schematic representation of the implemented ESD structure, on the right the leakage currents for both the single-sided as well as dual-sided ESD diode as a function of V_{GS}. The dual-sided ESD diode makes the transistor more suitable for applications that operate in Class-C and for applications that operate the transistor deep in saturation. In the case of a dual-sided ESD diode, no rectification will take place, and the V_{BIAS} remains constant under the most severe conditions.

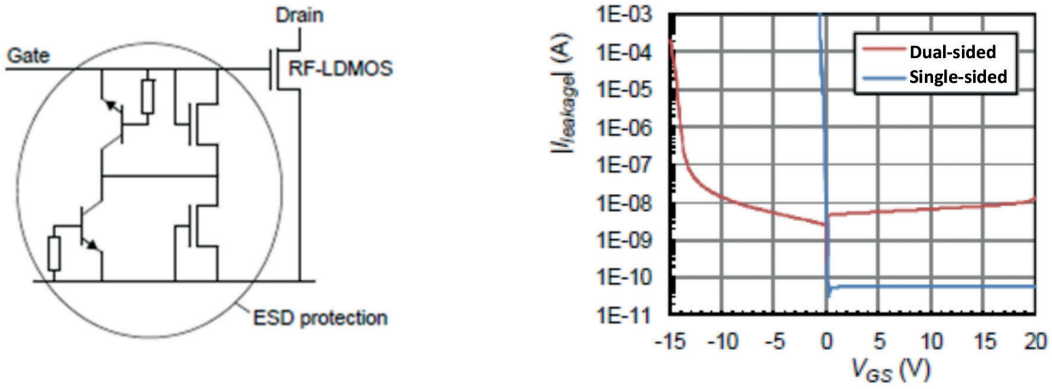


Figure 23: Schematic representation of the ESD diode implemented in the BLF18x-XR series and leakage characteristics of the single- and dual-sided ESD diode

Linearity

The BLF18x-XR transistor family is ideal for linear applications, with the internal die layout improved for linear operation. **Figure 24** shows the uncorrected linearity for a DVB-T signal at 225 MHz. On the left, the performance for a previous high voltage LDMOS generation is shown. On the right, uncorrected DVB-T shoulder performance is shown for the BLF18x-XR series. Shoulder improvements at lower power levels have been achieved, which makes it easy to pre-correct the transistor.

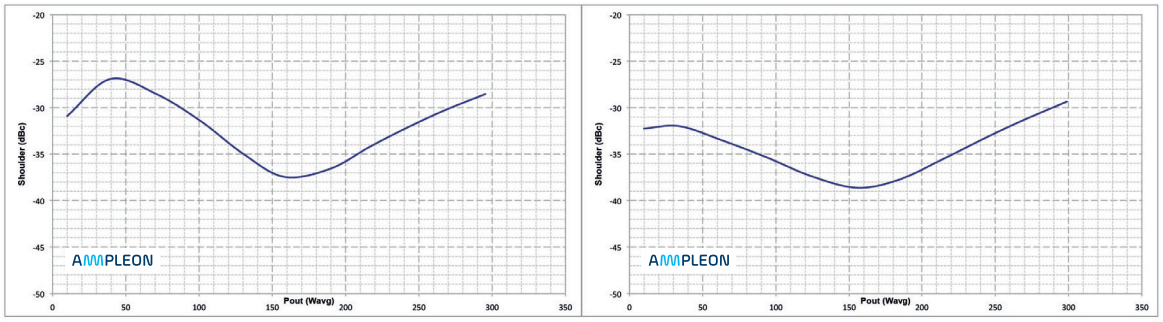


Figure 24: The BLF188XR (right) is extremely suited to linear applications. On the left an older LDMOS generation showing lower linearity at lower power levels, which can be more difficult to pre-correct

BLF18x-XR Series Reference Designs and Application Highlights

To support design-in activities a large variety of reference designs have been created. **Tables 4** and **5** give an overview of the designs that are currently available for the BLF184XR and BLF188XR, respectively. Four BLF188XR reference designs will be discussed in more detail. Extensive test reports including BOM, pc- board layout files and base plate drawings are available.

Test Signal	f (MHz)	V_{DS} (V)	P_{LOAD} (W)	Gain (dB)	Drain Eff. (%)
CW	88-108	50	740	21	83
	108-118	50	750	23.5	82

Table 4: BLF184XR reference designs

Test Signal	f (MHz)	V_{DS} (V)	P_{LOAD} (W)	Gain (dB)	Drain Eff. (%)
CW	Feb-30	50	1270	29.0	75
	27	50	1400	23.7	73
	41	50	1200	22.0	82
	60	48	1240	22.0	77
	72.5	50	1350	23.1	83
	81.4	50	1200	27.1	77.8
	88-108	45.5-47.5	1000	23.0	83.0
	88-108	50	1320	22.5	85
	108	50	1200	26.5	83
	200	50	1288	19.3	68.3
Pulsed CW	81.4	50	1200	25.8	85
	81.4	50	1400	25.4	81
	108	50	1400	24.0	73
DVB-T	174-230	50	225	23.8	29

Table 5: BLF188XR reference designs

BLF188XR Reference Design for 41 MHz

This 41 MHz reference design (see **Figure 25**) using the BLF188XR provides 1200 W output power with an efficiency of more than 80%. Its compact design (80 x 152 mm) features a 9:1 ferrite transformer on the input and a 4:1 coax transformer and balun on the output. **Figure 26** shows the RF performance. The reference design survives extreme mismatch conditions, as required in laser and plasma generator applications (see **Table 6**). A full description of this reference design can be found in **[5]**.

P_{LOAD} (W)	10:01	20:01	30:01:00	60:01:00	80:01:00	60-90:1
1000	pass	pass	pass	pass	pass	pass
1100	pass	pass	pass	pass	Pass	pass
1200	pass	pass	pass	pass	pass	pass

Table 6: VSWR test results BLF188XR at 41MHz
Test Conditions: Pulse width = 100 µsec, Duty cycle= 10 %
VSRW = 10:1 to 90:1, through all phases. V_{DS} = 50 Volts, I_{DQ} = 200 mA

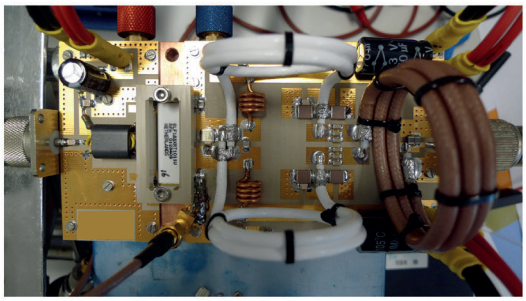


Figure 25: Compact BLF188XR 41 MHz reference design for laser and plasma applications

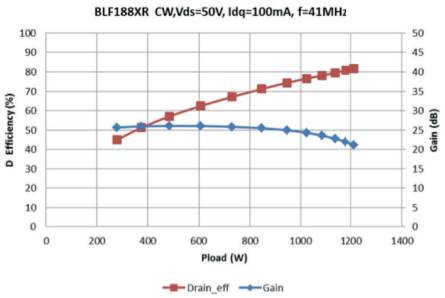


Figure 26: Continuous Wave performance of BLF188XR at 41 MHz

BLF188XR Reference Design for 81.36 MHz

This easy to reproduce reference design features an all planar matching structure (see **Figure 27**), eliminating the need for labor intensive coaxial transformers and baluns. The output power under pulsed conditions is 1400 W and the design can handle 1200 W continuous wave output power. See **Table 7** for a summary of the RF performance. The design is optimized for low spurious content under the most severe mismatch conditions. A full description of this reference design, including infrared scans of the matching structure under full CW operation, can be found in **[6]**.

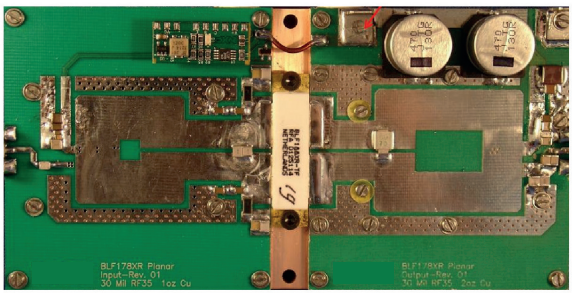


Figure 27: All planar reference design with the BLF188XR for 81.36 MHz

Symbol	Parameter	81.36 MHz Pulsed	81.36 MHz CW	Unit
V_{DS}	Power supply	50	50	V
I_{DQ}	Quiescent current	1000	1000	mA
PW	Pulse width	400	-	usec.
D/C	Duty Cycle	60	-	%
P_{out}	Output Power	1400	1200	W
G_p @P_{out}	Max power gain at P_{out}	25.4	27.1	dB
G_{comp}@P_{out}	Gain compression at P_{out}	2.6	0.8	dB
Eff @ P_{out}	Efficiency at Pout	81.0	77.8	%
2nd H	2nd Harmonic (100-1400 W output pwr.)	-26.4	-25.9	dBc
3rd H	3rd Harmonic (100-1400 W output pwr.)	-29.5	-29.5	dBc

Table 7: Performance summary BLF188XR at 81.36 MHz

BLF188XR for FM-broadcast 88-108 MHz

This FM broadcast (88-108 MHz) reference design with the BLF188XR features an even smaller planar matching structure at the input (see Figure 28), thus making the design even more compact. The planar impedance transformer can handle full continuous wave power in excess of 1200 W. **Figure 29** shows a thermal image of the output transformer at 1200 W continuous wave output power, with the hottest point in the entire circuit measuring 105 °C. Spurious content is suppressed by more than 60 dB under a VSWR = 5:1 at 1 kW continuous wave output power. In all cases the harmonic content is suppressed by more than 27 dB (1200 W CW into 50 Ohm load), see **Figure 30**. **Table 8** summarizes the RF performance of this FM broadcast demo, while a full description of the reference design can be found in **[7]**.

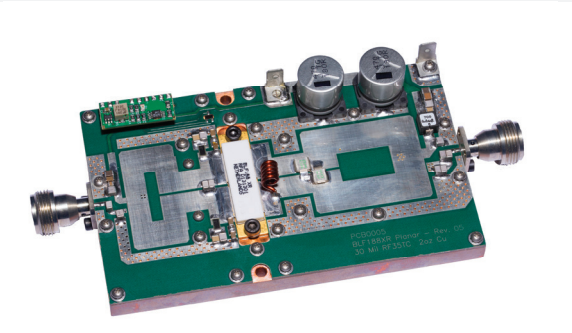


Figure 28: Compact, all planar, FM broadcast design with BLF188XR

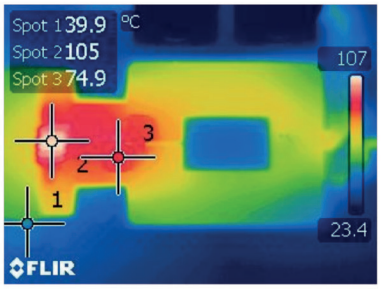


Figure 29: Thermal image of the output transformer of the BLF188XR FM design at 1200 W continuous wave output power

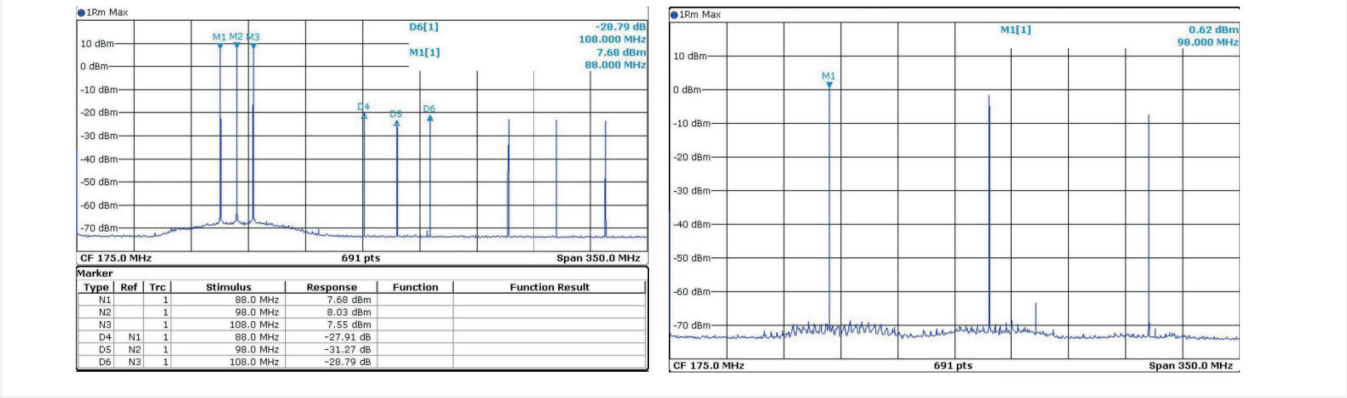


Figure 30: Harmonic content (left) up to 1200 W CW into 50 Ω is more than 27 dB suppressed. Spurious emission (right) is better than 60 dB under a 5:1 mismatch at 1 kW CW

Symbol	Parameter	88 MHz	98 MHz	108 MHz	Unit
I_{DQ}	Quiescent current	1000	1000	1000	mA
V_{DS}	Power supply	47.5	45.5	47.5	V
P_{out}	Peak Output power	1000	1000	1000	W
G @1000W	Gain at 1000 W Pout	23.0	23.3	23.1	dB
G_{comp} @1000W	Gain compression at 1000 W P_{out}	2.6	2.4	2.9	dB
Eff @1000W	Efficiency at 1000 W P_{out}	84.4	83.0	83.0	%
V_{DS}	Power supply	50	50	50	V
P_{out} @ P3dB	Peak Output power @ 3 dB gain comp.	1123	1227	1107	W
G @P3dB	Gain P3dB	22.8	22.9	23.0	dB
Eff @P3dB	Efficiency at P3dB	84.6	83.3	82.8	%
2nd H	2nd Harmonic (100-1000 W output pwr.)	-27.9	-31.3	-28.8	dBc
3rd H	3rd Harmonic (100-1000 W output pwr.)	-30.7	-31.5	-31.1	dBc

Table 8: Performance summary BLF188XR FM broadcast reference design

BLF188XR for VHF-TV 174-230 MHz

This reference design also features planar impedance transformers and provides optimum functionality with an ATSC, DVB-T, DVB-T2 or ISDB-T exciter. It delivers 225 W_{AVG} DVB-T power at -36 dBc shoulders (+/-4.3 MHz offset). **Figure 31** shows the pc-board layout. **Table 9** gives a summary of the performance, while **Table 10** shows the corrected DVB-T performance as a function of frequency and output power. Please note that the dissipated power in this reference is high, therefore a proper heat sink design is required. A full description of the reference design can be found in **[8]**.

Symbol	Parameter	Value	Unit
Freq.	Frequency Range	174-230	MHz
P_{out}	Average DVB-T output power	225	W
V_{DS}	Power supply	50	V
I_{DQ}	Quiescent drain current (total device)	2500	mA
P_{3dB}	Pulsed peak power 3 dB compression	1511	W
$ACPR_{Un\text{-}Corr.}$	DVB-T ACPR Un-Corrected @225 W	-30	dBc
$ACPR_{Corr.}$	DVB-T ACPR Corrected @225 W	-36	dBc
$Eff._{@225W}$	Minimum Efficiency at 225 W DVB-T Power	29	%
$Gmin._{@225W}$	Minimum DVB-T Gain at 225 W	23.8	dB
$G_{flatness}$	Gain flatness from 174 to 230 MHz at 225 W DVB-T power	0.7	dB

Table 9: Performance summary BLF188XR VHF-TV reference design

f (MHz)	DVB-T P_{OUT} (W)	DVB-T Gain (dB)	DVB-T Drain Eff (%)	DVB-T Corrected Shoulder (L/R)
174	200	24.4	27	-43 / -42
	225	24.4	29	-39 / -39
202	200	24.5	29	-41 / -43
	225	24.5	31	-37 / -41
230	200	23.9	29	-40 / -43
	225	23.8	31	-36 / -41

Table 10: Corrected DVB-T performance BLF188XR
Test conditions: V_{DS} = 50 V, I_{DQ} = 2500 mA, 8 MHz DVB-T signal, PAR = 9.2 dB @ 0.01% probability on the CCDF, Shoulder measured at +/- 4.3 MHz offset

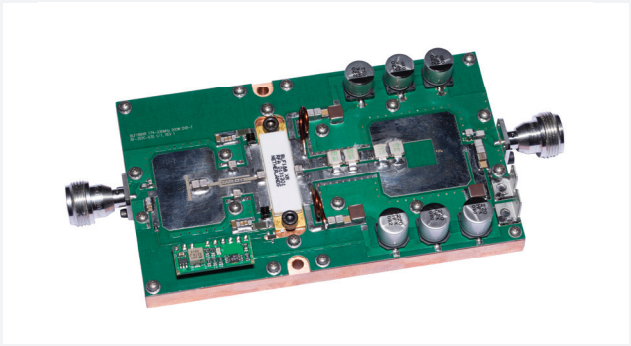


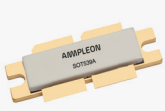
Figure 31: PC-board layout BLF188XR DVB-T reference design 174-230 MHz

Conclusions

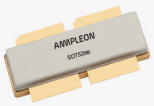
Ampleon has been the leader in ISM and broadcast RF Power transistors for the last 35 years. Its innovative High Voltage LDMOS technology enables ISM and broadcast RF power companies to design amplifiers with the industry's best reliability and performance. A small selection of the available reference designs for the BLF18x-XR-series has been discussed in more detail, providing RF power designers with an excellent starting point for their designs.

With the introduction of a complete BLF18x-XR-series product portfolio, Ampleon continues to demonstrate its leadership position in this market. As shown in this paper, the 50 V XR family clearly delivers the higher output power, easier design-in and lower system cost demanded by new demanding (kW) professional smart RF energy applications and terrestrial broadcasting designs.

Type Number	V_{DS} (V)	P_{OUT} (W)	Package	Status
BLF182XR	50	200	SOT1121A	Released
BLF182XRS	50	200	SOT1121B	Released
BLF183XR	50	300	SOT1121A	Released
BLF183XRS	50	300	SOT1121B	Released
BLF184XR	50	750	SOT1214A	Released
BLF184XRS	50	750	SOT1214B	Released
BLF188XR	50	1400	SOT539A	Released
BLF188XRS	50	1400	SOT539B	Released
BLF189XRA	50	1600	SOT539A	Q3-2017
BLF189XRB	50	1900	SOT539A	Q3-2017



SOT539A
41.2 x 10.2 x max 4.7 (mm))



SOT539B
(32.3 x 10.2 x max 4.7 (mm))

SOT1121A
(34.0 x 9.8 x max 4.7 (mm))

SOT1121B
(20.6 x 9.8 x max 4.7 (mm))

SOT1214A
(34.0 x 9.8 x max 4.7 (mm))

SOT1214B
(20.6 x 9.8 x max 4.7 (mm))

Table 11: 50 V Air-Cavity Ceramic Portfolio

Type Number	V_{DS} (V)	P_{OUT} (W)	Package	Status
BLP10H603	50	3	SOT1352-1	Released
BLP10H605	50	5	SOT1352-1	Released
BLP10H610	50	10	SOT1352-1	Released
BLP05H635XR	50	35	SOT1223-2	Released
BLP05H635XRG	50	35	SOT1224-2	Released
BLP05H675XR	50	75	SOT1223-2	Released
BLP05H675XRG	50	75	SOT1224-2	Released
BLP05H6110XR	50	110	SOT1223-2	Released
BLP05H6110XRG	50	110	SOT1224-2	Released
BLP05H6150XR	50	150	SOT1223-2	Released
BLP05H6150XRG	50	150	SOT1224-2	Released
BLP05H6250XR	50	250	SOT1223-2	Released
BLP05H6250XRG	50	250	SOT1224-2	Released
BLP05H6350XR	50	350	SOT1223-2	Released
BLP05H6350XRG	50	350	SOT1224-2	Released
BLP05H6700XR	50	700	SOT1138-2	Released
BLP05H6700XRG	50	700	SOT1204-2	Released

SOT1138-2
(20.6 x 10 x max 3.9 mm))

SOT1204-2
(20.6 x 10 x max 3.9 (mm))

SOT1223-2
(20.6 x 10 x max 3.9 (mm))

SOT1224-2
(20.6 x 10 x max 3.9 (mm))

SOT1352-1
(6 x 5 x max 1 (mm))

Table 12: 50 V Overmolded Plastic Portfolio

Acknowledgements

The authors would like to thank the members of the DTI-group, the R&D group, the members of the various global application teams and the marketing managers for their contributions to this paper.

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[7] Application Measurement Report; AR171052, BLF188XR, 88-108MHz. Please contact your Ampleon representative to obtain a copy of this report.

[8] Application Measurement Report; AR132170, BLF188XR Board 2323 VHF Band DVB-T. Please contact your Ampleon representative to obtain a copy of this report.

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